

IN THE CLAIMS:

Please amend claims 1-3, 6-9, 11, 13-15, and 21-25, as set forth below.

1 1. (Currently Amended) A method comprising:
2 depositing a layer of a metal on each of a number of conductors disposed on a surface of
3 a first wafer; and
4 forming a bond between the metal layer on one of ~~bonding~~ the conductors of the first
5 wafer ~~to~~ and one of a number of corresponding conductors on a surface of a
6 second wafer ~~using the metal layer~~.

1 2. (Currently Amended) The method of claim 1, further comprising, prior to
2 depositing the metal layer on each of the conductors, removing dielectric material from
3 the surface of the first wafer.

1 3. (Currently Amended) The method of claim 1, further comprising, prior to
2 depositing the metal layer on each of the conductors, removing native oxide from the
3 conductors.

1 4. (Original) The method of claim 1, wherein the conductors comprise
2 Copper.

1 5. (Original) The method of claim 1, wherein the metal comprises one of
2 Silver, Gold, Ruthenium, Osmium, Iridium, Palladium, Rhodium, and Platinum.

1 6. (Currently Amended) The method of claim 1, wherein the bond is formed
2 ~~bonding of the conductors of the wafer to the corresponding conductors of the second~~
3 ~~wafer is performed~~ at a temperature between approximately 100 and 300 degrees Celsius.

1 7. (Currently Amended) The method of claim 1, wherein depositing the
2 layer of metal on each of the conductors comprises:
3 forming a blanket layer of the metal over the conductors and the surface of the wafer; and
4 removing the metal from the wafer surfaces.

1 8. (Currently Amended) The method of claim 1, wherein depositing the
2 layer of metal on each of the conductors comprises selectively depositing the metal on
3 each of the conductors.

1 9. (Currently Amended) The method of claim 8, wherein selectively
2 depositing the metal on each of the conductors comprises one of an electroless plating
3 process, an electroplating process, and a contact displacement plating process.

1 10. (Original) The method of claim 1, wherein the metal layer on each of the
2 conductors comprises a number of islands.

1 11. (Currently Amended) The method of claim 10, wherein the islands are
2 selectively deposited on each of the conductors.

1 12. (Original) The method of claim 10, wherein the islands are formed by a
2 process comprising:
3 depositing a blanket layer of the metal over the conductors and the surface of the wafer;
4 and
5 removing the blanket metal layer from the wafer surface and from portions of each
6 conductor to form the number of islands on each conductor.

1 13. (Currently Amended) A method comprising:
2 depositing a layer of a first metal on each of a number of conductors disposed on a first
3 wafer;
4 depositing a layer of a second metal on each of a number of conductors disposed on a
5 second wafer;
6 aligning the first wafer with the second wafer; and
7 forming a bond between ~~bonding~~ the metal layer on one of the conductors of the first
8 wafer ~~with~~ and the metal layer on a mating one of the conductors of the second
9 wafer, wherein the bonded metal layers are disposed between the mating
10 conductors.

1 14. (Currently Amended) The method of claim 13, further comprising, prior
2 to depositing the metal layer on each of the conductors of at least one of the first and
3 second wafers, removing dielectric material from a surface of ~~each of the first and second~~
4 wafers the at least one wafer.

1 15. (Currently Amended) The method of claim 13, further comprising, prior
2 to depositing the metal layer on each of the conductors of at least one of the first and
3 second wafers, removing native oxide from the conductors of ~~each of the first and second~~
4 wafers the at least one wafer.

1 16. (Original) The method of claim 13, wherein the conductors of each of the
2 first and second wafers comprise the same metal.

1 17. (Original) The method of claim 16, wherein the conductors of each of the
2 first and second wafers comprise Copper.

1 18. (Original) The method of claim 13, wherein the first metal and the second
2 metal are the same.

1 19. (Original) The method of claim 13, wherein the first metal and the second
2 metal are different.

1 20. (Original) The method of claim 13, wherein each of the first and second
2 metals comprises one of Silver, Gold, Ruthenium, Osmium, Iridium, Palladium,
3 Rhodium, and Platinum.

1 21. (Currently Amended) The method of claim 13, wherein the bond is
2 formed ~~bonding of the conductors of the first wafer to the corresponding conductors of~~
3 ~~the second wafer is performed~~ at a temperature between approximately 100 and 300
4 degrees Celsius.

1 22. (Currently Amended) The method of claim 13, wherein depositing the
2 metal layer on each of the conductors of ~~each~~ at least one of the first and second wafers
3 comprises:
4 forming a blanket metal layer over the conductors and a surface of the wafer; and
5 removing the blanket metal layer from the wafer surface.

1 23. (Currently Amended) The method of claim 13, wherein depositing the
2 metal layer on each of the conductors of ~~each~~ at least one of the first and second wafers
3 comprises selectively depositing the metal layer on the conductors.

1 24. (Currently Amended) The method of claim 23, wherein selectively
2 depositing the metal layer on each of the conductors comprises one of an electroless
3 plating process, an electroplating process, and a contact displacement plating process.

1 25. (Currently Amended) The method of claim 13, wherein the metal layer on
2 each of the conductors of at least one of the first and second wafers comprises a number
3 of islands.

1 26. (Original) The method of claim 25, wherein the islands are selectively
2 deposited on the conductors.

1 27. (Original) The method of claim 25, wherein the islands are formed by a
2 process comprising:
3 depositing a blanket metal layer over each of the conductors and a surface of the wafer;
4 and
5 removing the blanket metal layer from the wafer surface and from portions of each
6 conductor to form the number of islands on each conductor.

1 28. (Withdrawn) A wafer stack comprising:
2 a first wafer including a number of conductors disposed on a surface of the first wafer,
3 each of the conductors having a layer of metal formed thereon; and
4 a second wafer including a number of conductors disposed on a surface of the second
5 wafer, each of the conductors having a layer of metal formed thereon;
6 wherein the metal layer of each conductor of the first wafer is bonded to the metal layer
7 on a corresponding conductor of the second wafer.

1 29. (Withdrawn) The wafer stack of claim 28, wherein the conductors on
2 each of the first and second wafers comprise the same metal.

1 30. (Withdrawn) The wafer stack of claim 29, wherein the conductors on
2 each of the first and second wafers comprise Copper.

1 31. (Withdrawn) The wafer stack of claim 28, wherein the metal layer on
2 each conductor of the first wafer and the metal layer on each conductor of the second
3 wafer comprises the same metal.

1 32. (Withdrawn) The wafer stack of claim 28, wherein the metal layer on
2 each conductor of the first wafer comprises a first metal and the metal layer on each
3 conductor of the second wafer comprises a second, different metal.

1 33. (Withdrawn) The wafer stack of claim 28, wherein the metal layer on
2 each conductor on each of the first and second wafers comprises one of Silver, Gold,
3 Ruthenium, Osmium, Iridium, Palladium, Rhodium, and Platinum.

1 34. (Withdrawn) The wafer stack of claim 28, wherein the first and second
2 wafers comprise the same material.

1 35. (Withdrawn) The wafer stack of claim 28, wherein the first wafer
2 comprises one material and the second wafer comprises a different material.

1 36. (Withdrawn) The wafer stack of claim 28, wherein the first wafer
2 includes logic circuitry and the second wafer includes memory circuitry.

1 37. (Withdrawn) A wafer stack comprising:
2 a first wafer, the first wafer having an interconnect including an uppermost dielectric
3 layer and a number of lower dielectric layers, each lower dielectric layer
4 including a number of conductors comprised of a first metal and the uppermost
5 dielectric layer including a number of conductors comprised of a third metal; and
6 a second wafer, the second wafer having an interconnect including an uppermost
7 dielectric layer and a number of lower dielectric layers, each lower dielectric layer
8 including a number of conductors comprised of a second metal and the uppermost
9 dielectric layer including a number of conductors comprised of a fourth metal;
10 wherein the conductors comprised of the third metal and the conductors comprised of the
11 fourth metal are capable of bonding together at a temperature of approximately
12 300° Celsius or less; and
13 wherein the conductors of the uppermost dielectric layer of the first wafer are bonded to
14 the conductors of the uppermost dielectric layer of the second wafer.

1 38. (Withdrawn) The wafer stack of claim 37, wherein the first and second
2 metals comprise the same metal.

1 39. (Withdrawn) The wafer stack of claim 38, wherein the first and second
2 metals comprise Copper.

1 40. (Withdrawn) The wafer stack of claim 37, wherein the third and fourth
2 metals comprise the same metal.

1 41. (Withdrawn) The wafer stack of claim 37, wherein each of the third and
2 fourth metals comprise one of Silver, Gold, Ruthenium, Osmium, Iridium, Palladium,
3 Rhodium, Platinum.

1 42. (Withdrawn) The wafer stack of claim 37, wherein the third metal
2 comprises one of Silver, Gold, Ruthenium, Osmium, Iridium, Palladium, Rhodium,
3 Platinum and the fourth metal comprises Copper.